What is claimed is:

1. An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a transfer circuit for receiving the first input signal and outputting a transfer circuit output signal having the same logical level as the first input signal; and

a control circuit, connected to the differential amplifier circuit and the transfer circuit, for selectively enabling the differential amplifier circuit and the transfer circuit in accordance with a control signal.

2. The input buffer circuit according to claim 1, wherein the control circuit enables the differential amplifier circuit and disables the transfer circuit when the first and second input signals have small amplitudes.

3. The input buffer circuit according to claim 2, wherein the control circuit disables the differential amplifier circuit and enables the transfer circuit when the first and second input signals have full amplitudes.

4. The input buffer circuit according to claim 1, wherein the differential amplifier circuit includes a constant current circuit and the control circuit disables the differential amplifier circuit by stopping a current from flowing through the constant current circuit.

5. The input buffer circuit according to claim 4, wherein the constant current circuit includes a constant current transistor and the control circuit disables the

differential amplifier circuit by turning off the constant current transistor.

6. The input buffer circuit according to claim 5, wherein the constant current transistor is turned off by the control circuit by applying the control signal at its gate.

7. The input buffer circuit according to claim 1, further comprising a driver circuit, connected to the differential amplifier circuit and the transfer circuit, for receiving the amplified signal from the differential amplifier circuit when the amplifier circuit is enabled and the transfer circuit output signal when the transfer circuit is enabled.

8. The input buffer circuit according to claim 7, wherein the control circuit includes an output selecting circuit for selecting either the amplified signal from the enabled differential amplifier circuit or the transfer circuit output signal from the enabled transfer circuit in accordance with the control signal and supplying the selected signal to the driver circuit.

9. The input buffer circuit according to claim 8, wherein the output selecting circuit includes a first transistor connected between the differential amplifier circuit and the driver circuit and a second transistor connected between the transfer circuit and the driver circuit, and the first and second transistors are of different conductivity types and are controlled by the control signal.

10. The input buffer circuit according to claim 8, wherein the output selecting circuit includes a first tri-

state inverter circuit, connected between the differential amplifier circuit and the driver circuit, for receiving the amplified signal from the differential amplifier circuit and a second tri-state inverter circuit, connected to the transfer circuit, for receiving the transfer circuit output signal, wherein the first and second tri-state inverter circuits are complimentarily set to a floating state in accordance with the control signal.

11. An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first tri-state inverter circuit, connected to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second tri-state inverter circuit for receiving the first input signal; and

a control circuit, connected to the differential amplifier circuit and the first and second tri-state inverter circuits, for selectively enabling the differential amplifier circuit and the first and second tri-state inverter circuits in accordance with a control signal.

12. The input buffer circuit according to claim 11, wherein the control circuit enables the differential amplifier circuit and the first tri-state inverter circuit and disables the second tri-state inverter circuit when the first and second input signals have small amplitudes.

13. The input buffer circuit according to claim 12, wherein the control circuit disables the differential amplifier circuit and the first tri-state inverter circuit

and enables the second tri-state inverter circuit when the first and second input signals have full amplitudes.

14. The input buffer circuit according to claim 11, further comprising a driver circuit, connected to the first and second tri-state inverter circuits, for receiving an output signal from the enabled one of the first and second tri-state inverter circuits enabled by the control circuit.

15. The input buffer circuit according to claim 11, wherein each of the first and second tri-state inverter circuits includes:

an inverter;

a PMOS transistor connected between the inverter and a high-potential power supply; and

an NMOS transistor connected between the inverter and a low-potential power supply.

16. The input buffer circuit according to claim 15, wherein the control circuit generates first and second control signals which are complementary each other, and wherein the PMOS transistor of the first tri-state inverter circuit and the NMOS transistor of the second tri-state inverter circuit are controlled by the first control signal and the NMOS transistor of the first tri-state inverter circuit and the PMOS transistor of the second tri-state inverter circuit are controlled by the second control signal.

17. A method of testing a semiconductor device, the semiconductor device including an output buffer connected between an internal logic circuit and a device pad, and an input buffer connected between the internal logic circuit and the device pad, and wherein the input buffer includes a

differential amplifier circuit for selectively amplifying an input signal thereto and a transfer circuit, the method comprising the steps of:

connecting a terminal resistor between the device pad and a high potential power supply;

supplying the input signal to the input buffer from the output buffer, wherein the differential amplifier circuit of the input buffer generates an amplified input signal and the transfer circuit of the input buffer generates a transfer signal having the same logic level as the input signal; and

providing a control signal to the input buffer to enable the differential amplifier circuit and disable the transfer circuit.

18. The method of claim 17, wherein the input signal has a small amplitude.